



Photo-ASIC based on Active Pixel Matrix

General Description

The Photo-ASIC based on an active pixel matrix, which is the core of an imager, is a mixed analog-digital circuit combining all of the followings elements on a single chip: Active Pixel Sensor (APS), ADC, logic-control blocks, FIFO, drivers, peripheral interfaces, EEPROM, etc. Such a circuit, integrated in a standard low-voltage CMOS process, is suited for cost-effective imaging applications. Ultra-low power consumption (typically 5 mW) allows the use of this type of device in battery-powered systems.

Technical Specifications – Basic Features

The CHIP

Power consumption	Typically 5 mW
Voltage supply range	2.7 – 3.3 V
Exposure time range	few μ s - 512 ms
Standby mode	

SENSOR

Pixel size	15 x 15 μ m ² , 8 x 8 μ m ²
High dynamic range response	Linear or logarithmic
Read out	Serial and/or parallel

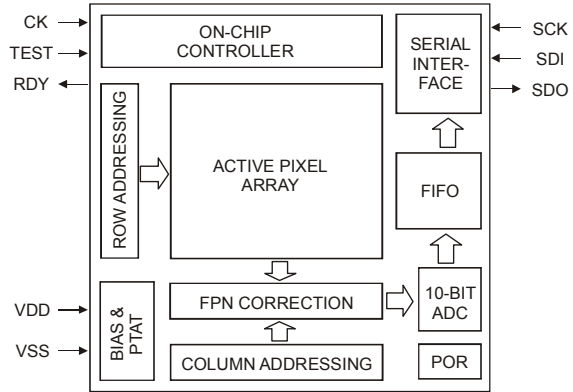
A/D CONVERTER

Resolution	up to 10 bit
Nominal sampling rate	1.2 MHz
Differential Non Linearity	\pm 0.5 LSB
Integral Non Linearity	\pm 0.9 LSB
SNR/SNDR	58.2 / 55 dB

Typical Applications

- Security
- Inspection systems
- Toys
- Ultra-low power imaging devices
- Automotive industry
- Machine vision
- Characters and patterns recognition

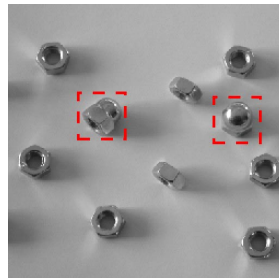
Typical Block Diagram



Key Features

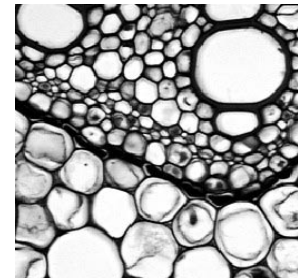
- Ultra low power consumption 5mW
- On-chip image pre-processing
- Serial interface (SPI)
- On-chip A/D converter
- Up to about 100K Active Pixels (APS)
- On-chip oscillator
- Up to 30 frames/s operation
- Dedicated exposure controller
- Drivers for peripherals
- 3V operation

Machine Vision



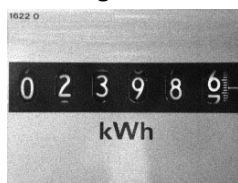
256x256 pixel array

Scientific Imaging

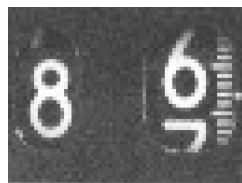


256x256 pixel array
(Image of vegetable tissue)

Metering – Pattern Recognition



256x192 pixel array



64x48 pixel array



32x24 pixel array